

METHOD OF FORMING A POLYSILICON RESISTOR

DESCRIPTION

Background of Invention

[Para 1] 1. Field of the Invention

[Para 2] The present invention relates to a method of forming a polysilicon resistor, and more particularly, to a method of forming a polysilicon resistor capable of providing a stable value of high resistance.

[Para 3] 2. Description of the Prior Art

[Para 4] In a semiconductor process, polysilicon is often positioned to function as resistors capable of providing high resistance. These resistors can be used in place of load transistors. When load transistors of a static random access memory (SRAM) is replaced by polysilicon resistors, the number of transistors in the SRAM can be reduced and thus saves cost and enhance the integration of the SRAM.

[Para 5] Referring to Figs. 1–3, Figs. 1–3 are schematic diagrams of a method of forming a polysilicon resistor according to the prior art. As shown in Fig. 1, a substrate 10 is provided. A dielectric layer 12 and a polysilicon layer 14 are formed on the substrate 10, respectively. Then, as shown in Fig. 2, a photolithographic process and an etching process are performed to remove portions of the polysilicon layer 14 and the dielectric layer 12 down to the surface of the substrate 10, thus defining the pattern of the polysilicon resistor. Normally, the polysilicon resistor has a sandwich-like structure that

sandwiches a high resistance polysilicon region between two low resistance polysilicon ends. The low resistance polysilicon ends are provided for forming interconnection contact plugs to connect the polysilicon resistor with other wirings. The high resistance polysilicon region is used to provide a high resistance to satisfy circuit designs or device demands.

[Para 6] As shown in Fig. 3, the resistance at different regions of the polysilicon resistor is now adjusted to define the high resistance region and the low resistance regions at both sides of the high resistance region. For example, a photolithographic process is performed to form a mask layer 16 on the polysilicon layer 14 to cover the region for forming the high resistance region. Following that, an ion implantation process is performed using N-type or P-type dopants to dope the portions of the polysilicon layer 14 not covered by the mask layer 16, thus reducing the resistance of the portions of the polysilicon layer 14 at the either side of the high resistance region. Since the portions of the polysilicon layer 14 in the undoped region has higher resistance than the portions of the polysilicon layer 14 in the doped region, the high resistance region and the low resistance regions are now defined to complete the fabrication of the polysilicon resistor. In order to satisfy the electrical characteristics demands of the products, sometimes a lightly doping process (such as an N- doping or P- doping) is used to dope the entire surface of the polysilicon layer 14, including the low resistance regions and the high resistance region. Following that, a heavily doping process (such as an N+ doping or P+ doping) is performed using the same type dopants to dope the portions of the polysilicon layer 14 at the low resistance regions.

[Para 7] With the development of the various electronic products, circuit designs applying polysilicon resistors to replace load resistors become more and more complicated. For example, for the analog/digital mixed mode integrated circuits or the radio frequency integrated circuits, it is required that the load resistors have a high value of ohmic resistance and the value of the ohmic resistance must further be within tight limits. Therefore, how to

produce load resistors with a stable value of high resistance and decrease cross section areas of the load resistors for enhancing the device integration are very important for the application of the polysilicon resistors.

Summary of Invention

[Para 8] It is therefore an object of the claimed invention to providing a method of forming a polysilicon resistor capable of providing a stable value of high resistance.

[Para 9] According to the claimed invention, a polysilicon layer is formed on a dielectric layer positioned on a substrate. Then, the polysilicon layer is doped with first type dopants and second type dopants. Portions of the polysilicon layer and the dielectric layer are removed down to the surface of the substrate, so as to define at least a high resistance region and a low resistance region on the remainder of the polysilicon layer. Finally, a salicide layer is formed on the portions of the polysilicon layer within the low resistance region.

[Para 10] It is an advantage of the present invention that the first type dopants and the second type dopants are used to adjust the resistance of the portions of the polysilicon layer within the high resistance region. Being controlled by the dosage adjustment of the first type dopants and the second type dopants, a uniform and stable value of high resistance is therefore obtained to satisfy the circuit designs. In this case, a cross section area of the polysilicon resistor can also be reduced to enhance the device integration.

[Para 11] These and other objects of the claimed invention will be apparent to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[Para 12] Figs. 1–3 are schematic diagrams of a method of forming a polysilicon resistor according to the prior art; and

[Para 13] Figs. 4–9 are schematic diagrams of a method of forming a polysilicon resistor according to the present invention.

Detailed Description

[Para 14] Referring to Figs. 4–9, Figs. 4–9 are schematic diagrams of a method of forming a polysilicon resistor according to the present invention. As shown in Fig. 4, a dielectric layer 22 and a polysilicon layer 24 are formed on a substrate 20, respectively. Following that, as shown in Fig. 5, an ion implantation process is performed using both of N-type dopants and P-type dopants to dope the polysilicon layer 24, thus adjusting the resistance of the polysilicon layer 24. In a better embodiment of the present invention, a dosage of the N-type dopants and a dosage of the P-type dopants have the same order of magnitude. For example, the N-type dopants can be As⁻ ions with a dosage of approximate 3E15, and the P-type dopants can be BF₂⁺ ions with a dosage of approximate 1.5E15. However, the present invention is not limited, other N-type dopants (such as P or Sb) and P-type dopants (such as Ge or B) having the same order of magnitude can also be applied in the present invention to adjust the resistance of the polysilicon layer 24. When a cross section area of the polysilicon layer 24 of 100μm x 10μm is suggested, a high resistance value of approximate 29kohm/sq for the polysilicon layer 24 can be obtained. Since the variance for 25 wafers is measured to below 5%, an excellent uniformity in the polysilicon resistors can also be obtained according to the present invention.

[Para 15] As shown in Fig. 6, a photolithographic process and an etching process are then used to remove portions of the polysilicon layer 24 and the

dielectric layer 22 down to the surface of the substrate 20, thus defining the pattern of the polysilicon resistor. Alternatively, the pattern of the polysilicon resistor can be defined using the photolithographic process and the etching process prior to the ion implantation process using both of the N-type dopants and the P-type dopants for adjusting the resistance of the polysilicon layer 24.

[Para 16] As shown in Fig. 7, a high resistance region 26 is defined at a central region of the polysilicon layer 24, and at least a low resistance region 28 is defined at the either side of the high resistance region 26. Following that, a salicide block (SAB) 30 is formed on the portions of the polysilicon layer 24 within the high resistance region 26. Using the SAB 30 as a mask, a salicide layer 32 is formed on the portions of the polysilicon layer 24 within the low resistance region 28. An example of the methods of forming the SAB 30 and the salicide layer 32 is further explained below. A dielectric layer (not shown) is deposited on the surface of the substrate 20 followed by using a photolithographic process and an etching process to completely remove the portions of the dielectric layer in the low resistance region 28, thus forming the SAB 30 by the remainder of the dielectric layer in the high resistance region 26. Subsequently, a salicide process is performed by first using a physical vapor deposition (PVD) method to sputter a metal layer (not shown) on the surface of the substrate 20. The metal layer is composed of tungsten or titanium. A thermal treatment process is thereafter performed to allow the reaction of the metal layer with the portions of the polysilicon layer 24 in the low resistance region 28, thus forming the salicide layer 32.

[Para 17] In a better embodiment of the present invention, the polysilicon resistor has a sandwich-like structure which sandwiches the high resistance region 26 for providing high resistance between two low resistance regions 28 for forming the interconnection contact plugs. The present invention is characterized by using two different types of dopants to adjust the polysilicon resistance in the high resistance region, and forming the salicide

layer to reduce the polysilicon resistance in the low resistance region. Therefore, the present invention is not limited to the sandwich-like polysilicon resistor, and can also be applied in the polysilicon resistors of other structures to adjust the polysilicon resistance thereof.

[Para 18] Figs. 8 and 9 illustrate a method of forming an interconnection between the polysilicon resistor and other wirings. As shown in Fig. 8 and Fig. 9, an inter layer dielectric (ILD) 34, such as a silicon oxide layer or a borophosphosilicate glass (BPSG), is formed on the surface of the substrate 20 to insulate the salicide layer 32 from other conductive materials. Following that, a photolithographic process and an etching process are performed to form at least a contact hole 36 in the inter layer dielectric 34 to connect to the salicide layer 32. A conductive layer 38 is then formed on portions of the inter layer dielectric 34 and within the contact hole 36, thus connecting the polysilicon resistor to wirings formed above the inter layer dielectric 34 via the conductive layer 38 filling in the contact hole 36.

[Para 19] In contrast to the prior art method of forming the polysilicon resistor, the present invention uses two different types of dopants to adjust the polysilicon resistance in the high resistance region. Being controlled by the dosage of the dopants, the polysilicon resistance in the high resistance region has a value ranging between ten and thousands kohm/sq according to the present invention. Therefore, the polysilicon resistor of the present invention is capable of providing a uniform and stable value of high resistance to satisfy the high resistance requirements for the SRAM, analog, digital/analog mixed mode and radio frequency circuit designs. In this case, a cross section area of the polysilicon resistor can also be reduced to enhance the device integration.

[Para 20] Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the

teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.